AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method for processing cache memory accesses in a computing system having a requester to submit memory access addresses for requested data, and having a tag memory to store tag addresses corresponding to addresses stored in the cache memory, the method comprising:

retrieving a stored tag address from the tag memory in response to the requester submitting a memory access address;

performing a first comparison of only the memory access address to the stored tag address, without regard to any error correction code associated with the stored tag address, to determine whether the requested data is stored in the cache memory and storing in a first latch a result of the first comparison;

monitoring for an error in the stored tag address contemporaneously with the first comparison of the memory access address and the stored tag address and storing in a second latch a result of the monitoring for errors, wherein monitoring for errors in the stored tag address comprises identifying at least one error using a single error correction code associated with the stored tag address in the tag memory, wherein the single error correction code is coded to provide error detection for the stored tag address and a plurality of configuration fields;

if a tag address error is detected in the stored tag address, blocking output from the first latch in response to output from the second latch, correcting the tag address error using an error correction code associated with the stored tag address, and performing a second comparison of the memory access address and the corrected tag address to determine whether the requested data is stored in the cache memory, wherein the second comparison compares only the corrected tag address with the memory access address, and disregards comparison of any stored error correction code bits; and

if no tag address error is detected in the stored tag address, passing output from the first latch in response to output from the second latch to determine whether the requested data is stored in the cache memory.

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (previously presented) The method of Claim 1, wherein performing the first comparison and monitoring for errors in the stored tag address occur in parallel with correcting the tag address error and performing the second comparison.

7. (original) The method of Claim 1, wherein correcting the tag address error and performing the second comparison are initiated upon recognition of a tag address error.

8. (original) The method of Claim 1, wherein disregarding the first comparison comprises blocking passage of the results of the first comparison through an output gate.

9. (original) The method of Claim 8, wherein blocking passage of the first comparison results comprises:

providing an error signal to the output gate when a tag address error is detected; and

disabling an output of the output gate upon receipt of the error signal.

10. (previously presented) The method of Claim 9, further comprising enabling the tag address error to be corrected and the second comparison of the memory access address and corrected tag addresses to be performed in response to the error signal.

11. (currently amended) A cache hit detector, comprising:

(a) a tag memory to store tag addresses corresponding to addresses currently cached, and further to store an error correction code for each block of data stored in the tag memory, wherein each block of data is associated with a single error correction code, and the single error correction code provides error correction capabilities for the stored tag address and a plurality of configuration fields;

(b) a fast hit detection circuit, comprising:

(i) a first address compare module coupled to the tag memory to receive a tag address and to compare only the tag address to a requested address without involving the error correction code in the comparison;

(ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address;

(iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if the requested address is stored in the tag memory as determined by the comparison of only the tag address and the requested address, and if and only if no error is discovered by the error detector;

(iv) a first latch coupled to the first address compare module to latch comparison results;

(v) a second latch coupled to the error detector to latch a resulting error indicator signal; and

wherein the comparison results and the error indicator signal are not passed to the gated output until both the comparison results and the error indicator signal are available at the first and second latches, and until simultaneously clocked to concurrently provide the comparison results and the error indicator signal to the gated output; and

(c) a slow hit detection circuit, comprising:

(i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address; and

(ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare only the corrected tag address to address without involving any error correction code in the comparison.

12. (original) The cache hit detector as in Claim 11, wherein the fast hit detection circuit and the slow hit detection circuit are coupled in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit.

13. (original) The cache hit detector as in Claim 11, further comprising latching means to coordinate timing between the fast hit detection circuit and the slow hit detection circuit.

14. (canceled)

15. (original) The cache hit detector as in Claim 11, wherein the first address compare module and the error detector are coupled in parallel to contemporaneously compare the tag address to a requested address and determine whether there are any errors in the tag address.

16. (canceled)

17. (original) The cache hit detector as in Claim 11, wherein the error detector determines whether there are any single bit errors in the tag address.

18. (currently amended) A data processing system comprising:

(a) a main memory module for storing data;

(b) at least one cache memory coupled to the main memory module to cache at least a portion of the data stored in the main memory module;

(c) at least one processing unit to process data and to control data access with the main memory module and the cache memory, the processing unit comprising:

(1) a tag memory to store tag addresses corresponding to addresses currently cached, wherein the tag memory further stores an error correction code associated with each block of data, wherein each block of data is associated with a single error correction code, and the single error correction code provides error correction capabilities for the stored tag address and a plurality of configuration fields;

(2) a fast hit detection circuit, comprising:

(i) a first address compare module coupled to the tag memory to receive a tag address and to compare only the tag address to a requested address without involving the error correction code in the comparison;

(ii) an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address;

(iii) a gated output module coupled to the first address compare module and the error detector to output a fast hit indication if the requested address is stored in the tag memory as determined by the comparison of only the tag address and the requested address, and if and only if no error is discovered by the error detector;

(iv) a first latch coupled to the first address compare module to latch comparison results;

(v) a second latch coupled to the error detector to latch a resulting error indicator signal; and

wherein the comparison results and the error indicator signal are not passed to the gated output until both the comparison results and the error indicator signal are available at the first and second latches, and until simultaneously clocked to concurrently provide the comparison results and the error indicator signal to the gated output; and

(3) a slow hit detection circuit, comprising:

(i) an error correction circuit coupled to the tag memory to receive the tag address and to correct errors in the tag address; and

(ii) a second address compare module coupled to the error correction circuit to receive the corrected tag address and to compare only the corrected tag address to the requested address without involving any error correction code in the comparison.

19. (original) The data processing system of Claim 18, wherein the fast hit detection circuit and the slow hit detection circuit are configured in parallel such that the first address compare module and the error detector perform operations concurrently with operations of the second address compare module and the error correction circuit.

20. (canceled)

21. (canceled)

22. (canceled)

23. (currently amended) An apparatus ~~method~~ for processing cache memory accesses in a computing system having a requester to submit memory access addresses for requested data, and having a tag memory to store tag addresses corresponding to addresses stored in the cache memory, the method comprising:

means for retrieving a stored tag address from the tag memory in response to the requester submitting a memory access address;

means for performing a first comparison of only the memory access address to the stored tag address, without regard to any error correction code associated with the stored tag address, to determine whether the requested data is stored in the cache memory and storing in a first latch a result of the first comparison;

means for monitoring for an error in the stored tag address contemporaneously with the first comparison of the memory access address and the stored tag address and storing in a second latch a result of the monitoring for errors, wherein the means for monitoring comprises means for identifying at least one error using a single error correction code associated with the stored tag

address in the tag memory, wherein the single error correction code is coded to provide error detection for the stored tag address and a plurality of configuration fields;

means, responsive to detection of a tag address error in the stored tag address, for blocking output from the first latch in response to output from the second latch, correcting the tag address error using an error correction code associated with the stored tag address, and performing a second comparison of the memory access address and the corrected tag address to determine whether the requested data is stored in the cache memory, wherein the second comparison compares only the corrected tag address with the memory access address and disregards comparison of any stored error correction code bits; and

means, responsive to no detection of a tag address error in the stored tag address, for enabling output from the first latch in response to output from the second latch to determine whether the requested data is stored in the cache memory.